

When you're done remember to save your work by clicking on the "Save" button at the bottom of the page. You can check if your answers are correct by clicking on the "Check" button.

## Lab 1: Terman, Chris

When entering numeric values in the answer fields, you can use integers (1000), floating-point numbers (1000.0), scientific notation (1e3), or JSim numeric scale factors (1K).

- (A) Report the mosfet  $I_{ds}$  you measured from the device curves for  $V_{gs} = 5V$  and  $V_{ds} = 1.2V$ .

**$I_{ds}$  (in amps):**

Compute the effective channel sheet resistance using  $(V_{ds})/(I_{ds})$  as an estimate for the channel resistance of the test mosfet. Don't forget to correct for the W/L of the test device!

**Sheet resistance (in ohms):**

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- (B) Report the mosfet  $I_{ds}$  you measured from the device curves for  $V_{gs} = 0V$  and  $V_{ds} = 2.5V$ .

**$I_{ds}$  (in amps):**

Calculate the time it would take to discharge 0.05pF capacitor from 5V to 2.5V.

**Discharge time (in seconds):**

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- (C) Determine a scaled width (SW) for the two pullup mosfets so that the  $V_{in}$  and  $V_{out}$  curves for the NAND gate intersect at  $V_{DD}/2$  (1.65V).

**Scaled width:**

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- (D) What is the largest noise immunity we could specify and still have the NAND gate qualify as a legal device? Please fill in your answer with a precision of .01 volts.

**Maximum noise immunity (in volts):**

Hint: to measure the low noise margin, use the VTC to determine what  $V_{in}$  has to be in order for  $V_{out}$  to be 3V, then subtract  $V_{ol}$  (0.3V) from that number. To measure the high noise margin, use the VTC to determine what  $V_{in}$  has to be in order for  $V_{out}$  to be 0.3V, then subtract that number from  $V_{oh}$  (3.0V).

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(E) Following standard practice, choose the logic thresholds as follows:

$$V_{ol} = 10\% \text{ of power supply voltage} = 0.3V$$

$$V_{il} = 20\% \text{ of power supply voltage} = 0.6V$$

$$V_{ih} = 80\% \text{ of power supply voltage} = 2.6V$$

$$V_{oh} = 90\% \text{ of power supply voltage} = 3.0V$$

Measure the contamination and propagation times for your NAND gate using both the falling and rising output transitions.

**$t_C$  for falling output (in seconds):**

**$t_P$  for falling output (in seconds):**

**Output fall time (in seconds):**

**$t_C$  for rising output (in seconds):**

**$t_P$  for rising output (in seconds):**

**Output rise time (in seconds):**

Use these measurements compute estimates for  $t_C$  and  $t_P$ .

**$t_C$  (in seconds):**

**$t_P$  (in seconds):**

(F) Recompute  $t_C$  and  $t_P$  using measurements at 0 degrees C and 100 degrees C.

**Recomputed  $t_C$  (in seconds):**

**Measurement used:**

**Recomputed  $t_P$  (in seconds):**

**Measurement used:**

**% change in  $t_P$ :**

(G) Compute derating factors for worst case and best case conditions.

**worst case derating factor:**

**best case derating factor:**

**derating factor, best case to worst case:**

(H) Compute extrinsic delay for falling and rising output transition. Remember to

convert the answer to the correct units!

**extrinsic delay, falling output (in ns/pf):**

**extrinsic delay, rising output (in ns/pf):**

Check

Save